XENPAK Dual SC Optical Transceivers

Introduction

This design guide provides the information needed to incorporate OptixCom's fiber optics transceiver products in the customer's system. Xenpak is a Multisource Agreement (MSA) that defines a fiber-optic or wired transceiver module which conforms to the 10 Gigabit Ethernet (10GbE) standard of the IEEE 802.3 working group. OptixCom's XENPAK series of the transceiver products are compliant with the XENPAK MSA. For more detail information, please refer to the URL http://207.158.200.152//SFP/SFP%20MSA.pdf or visit OptixCom web site: http://www.OptixCom.com for the official documentation.

The reference guide covers the following topics:

A.Pin Assignment & Description
B.Functional Diagram
C.Package Outline
D.Transceiver and Host Printed Circuit Board
E.Optical Interface
F.Mechanical Forces
G.Transceiver and Connector Durability
H.XENPAK Thermal Requirements
I.XENPAK Electrical Interface
J.Fixed Voltage Supply Specs and Inrush Currents
K.Transceiver Monitoring

A. Pin Assignment & Description

Pin No	Name	Dir	Function	Notes
1	GND		Electrical Ground	1
2	GND		Electrical Ground	1
3	GND		Electrical Ground	1
4	5.0V		Power	2
5	3.3V		Power	2
6	3.3V		Power	2
7	APS		Adaptive Power Supply	2
8	APS		Adaptive Power Supply	2
9	LASI		Open Drain Compatible 10K-22K pull up on host. Logic High: Normal Operation Logic Low: LASI Asserted	4
10	RESET	I	Open Drain compatible. 10-22K pull-up on transceiver Logic high = Normal operation Logic low = Reset Minimum reset assert time 1 ms	4
11	VEND SPECIFIC		Vendor Specific Pin. Leave unconnected when not in use.	8

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A. Pin Assignment & Description (Cont'd)

Pin No	Name	Dir	Function	Notes
12	TX ON/OFF	I	Open Drain compatible. 10-22K pull-up on transceiver Logic high = Transmitter On (capable) Logic low = Transmitter Off (always)	4
13	RESERVED		Reserved	4
14	MOD DETECT	O	Pulled low inside module through 1k	
15	VEND SPECIFIC		Vendor Specific Pin. Leave unconnected when not in use.	8
16	VEND SPECIFIC		Vendor Specific Pin. Leave unconnected when not in use.	8
17	MDIO	I/O	Management Data IO	4, 5
18	MDC	I	Management Data Clock	4, 5
19	PRTAD4	I	Port Address Bit 4 (Low = 0)	4
20	PRTAD3	I	Port Address Bit 3 (Low = 0)	4
21	PRTAD2	I	Port Address Bit 2 (Low = 0)	4
22	PRTAD1	I	Port Address Bit 1 (Low = 0)	4
23	PRTAD0	I	Port Address Bit 0 (Low = 0)	4
24	VEND SPECIFIC		Vendor Specific Pin. Leave unconnected when not in use.	8
25	APS SET		Feedback input for APS	
26	RESERVED		Reserved for Avalanche Photodiode use.	8
27	APS SENSE		APS Sense Connection	
28	APS		Adaptive Power Supply	2
29	APS		Adaptive Power Supply	2
30	3.3V		Power	2
31	3.3V		Power	2
32	5.0V		Power	2
33	GND		Electrical Ground	1
34	GND		Electrical Ground	1
35	GND		Electrical Ground	1
36	GND		Electrical Ground	1
37	GND		Electrical Ground	1
38	RESERVED		Reserved	
39	RESERVED		Reserved	
40	GND		Electrical Ground	1
41	RX LANE0+	O	Module XAUI Output Lane 0+	7
42	RX LANE0-	O	Module XAUI Output Lane 0-	7
43	GND		Electrical Ground	1
44	RX LANE1+	O	Module XAUI Output Lane 1+	7
45	RX LANE1-	O	Module XAUI Output Lane 1-	7
46	GND		Electrical Ground	1
47	RX LANE2+	O	Module XAUI Output Lane 2+	7
48	RX LANE2-	O	Module XAUI Output Lane 2-	7
49	GND		Electrical Ground	1
50	RX LANE3+	O	Module XAUI Output Lane 3+	7
51	RX LANE3-	O	Module XAUI Output Lane 3-	7
52	GND		Electrical Ground	1

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A. Pin Assignment & Description (Cont'd)

Pin No	Name	Dir	Function	Notes
53	GND		Electrical Ground	1
54	GND		Electrical Ground	1
55	TX LANE0+	I	Module XAUI Input Lane 0+	7
56	TX LANE0-	I	Module XAUI Input Lane 0-	7
57	GND		Electrical Ground	1
58	TX LANE1+	I	Module XAUI Input Lane 1+	7
59	TX LANE1-	I	Module XAUI Input Lane 1-	7
60	GND		Electrical Ground	1
61	TX LANE2+	I	Module XAUI Input Lane 2+	7
62	TX LANE2-	I	Module XAUI Input Lane 2-	7
63	GND		Electrical Ground	1
64	TX LANE3+	I	Module XAUI Input Lane 3+	7
65	TX LANE3-	I	Module XAUI Input Lane 3-	7
66	GND		Electrical Ground	1
67	RESERVED		Reserved	
68	RESERVED		Reserved	
69	GND		Electrical Ground	1
70	GND		Electrical Ground	1

Notes:

1) Ground connections are common for TX and RX.
2) All connector contacts are rated at 0.5A nominal.
3) 1.2V CMOS compatible.
4) MDIO and MDC timing must comply with IEEE802.3ae Clause 45.3.
5) XAUI output characteristics should comply with IEEE802.3ae Clause 47.
6) Transceivers will be MSA compliant when no signals are present on the vendor specific pins.

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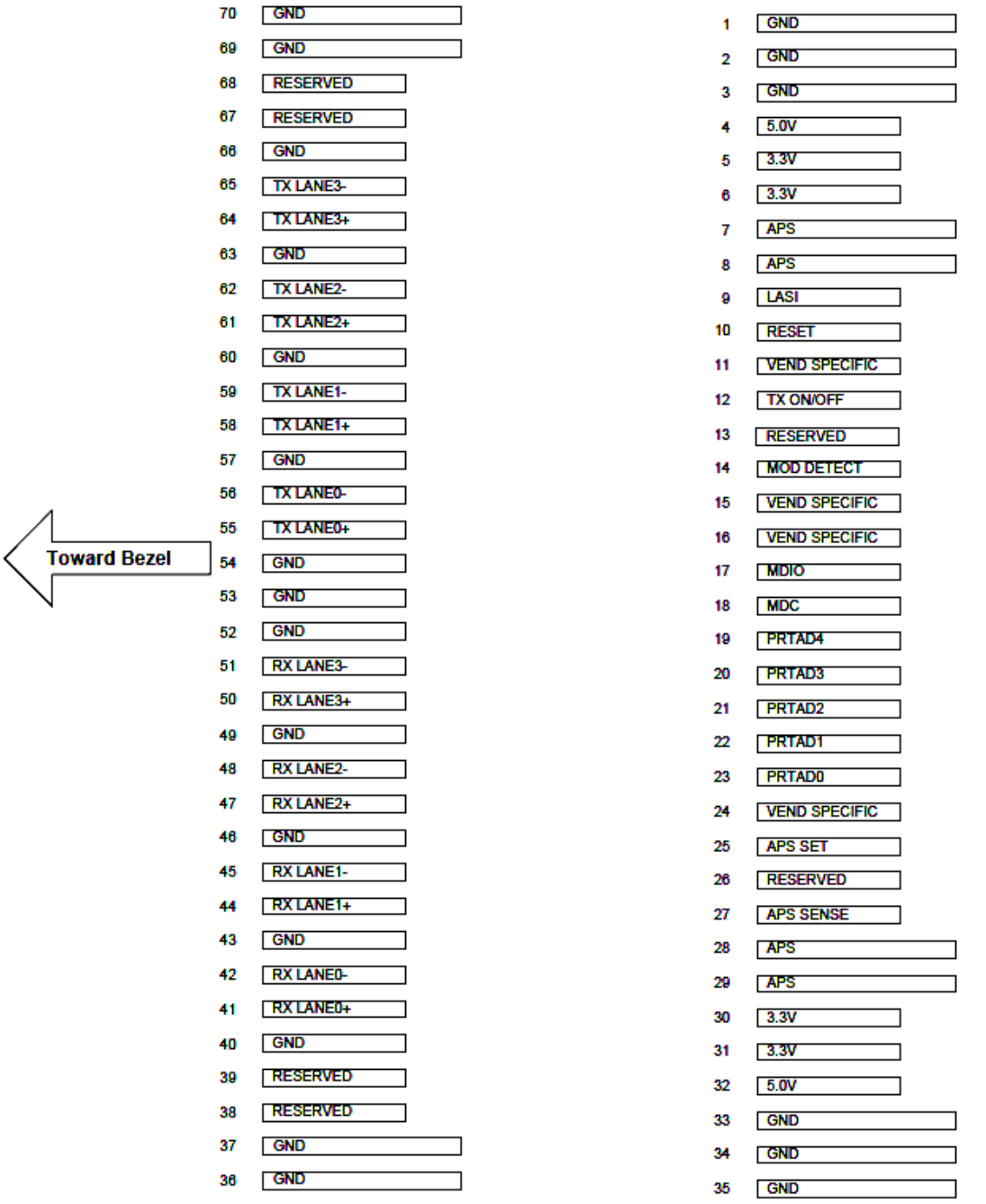
XENPAK Transceiver Pad Layout



Top of Transceiver PCB **Bottom of Transceiver PCB**

(As viewed through top)

Ground Pins 1,2,3,33,34,35,36,37,69,70 and APS power pins 7,8,28,29, are extended so as to make contact first upon XENPAK insertion.

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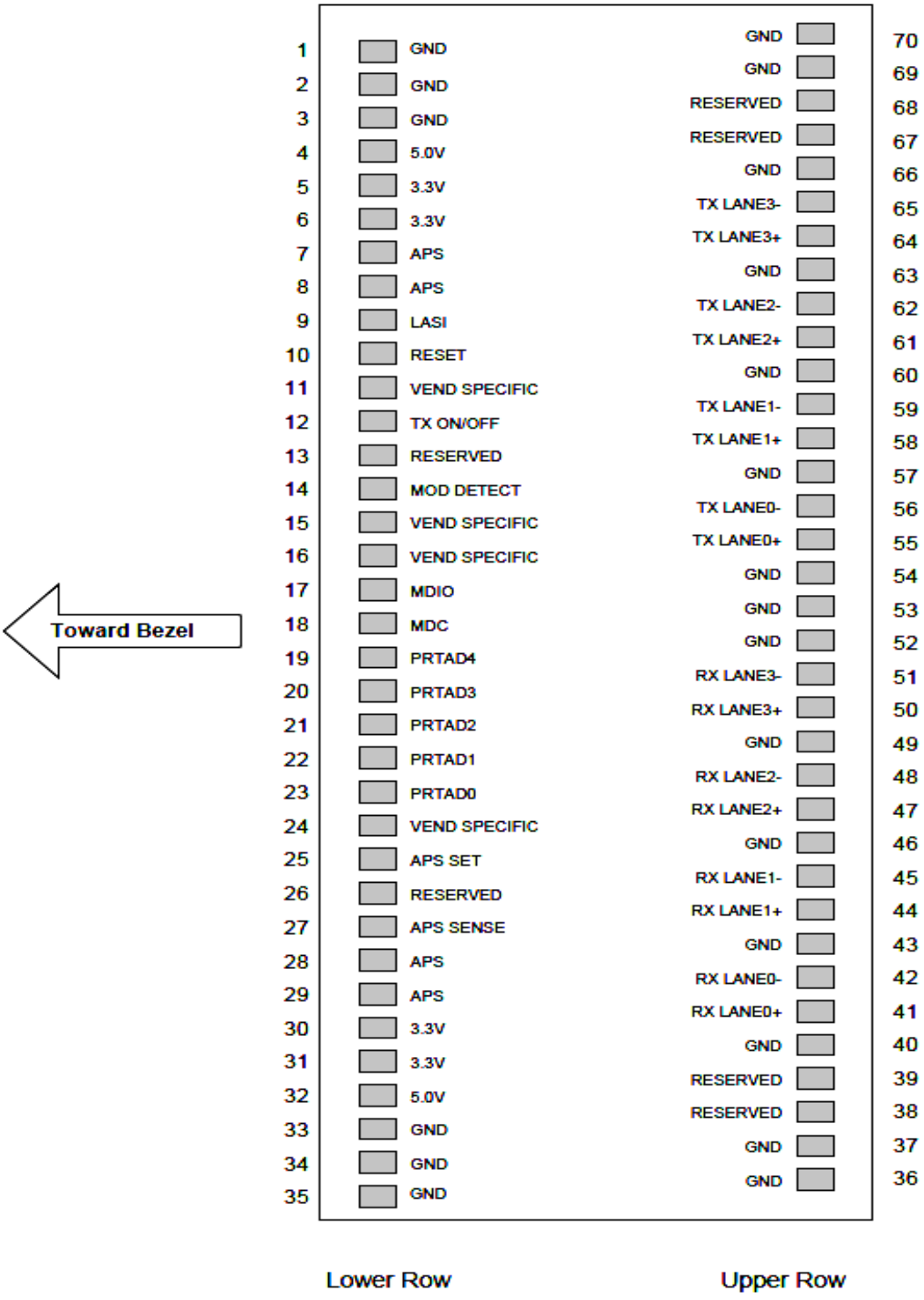
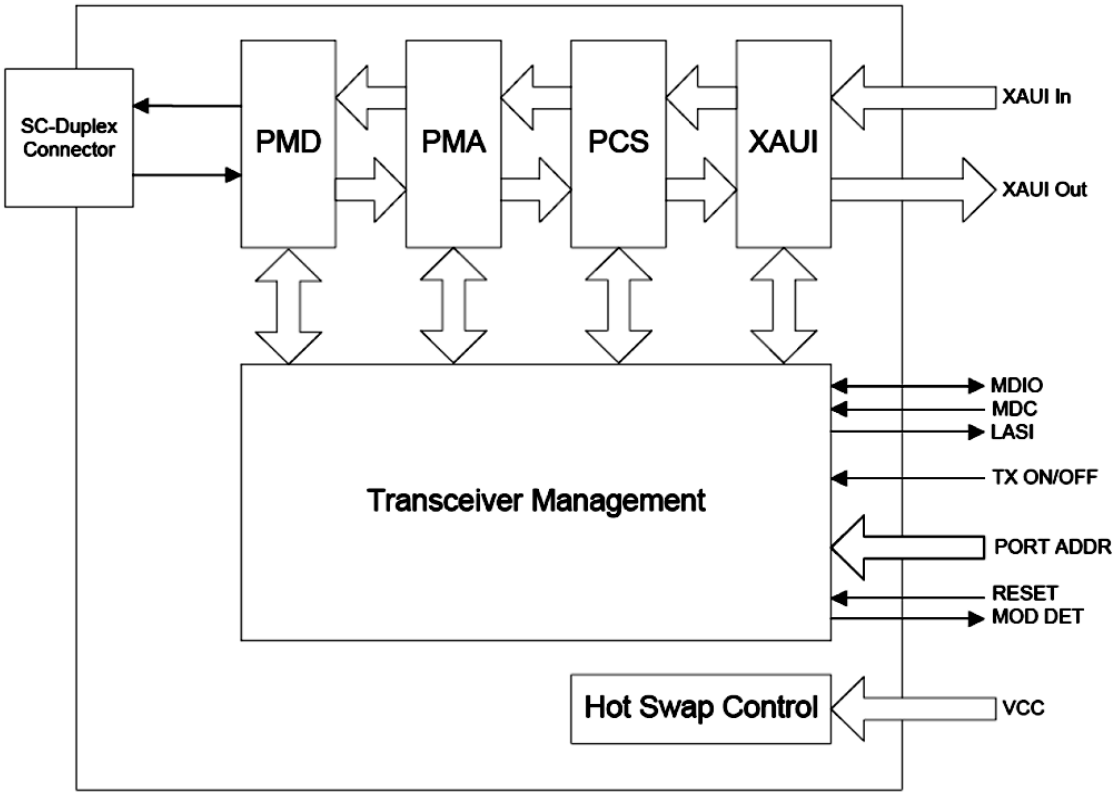
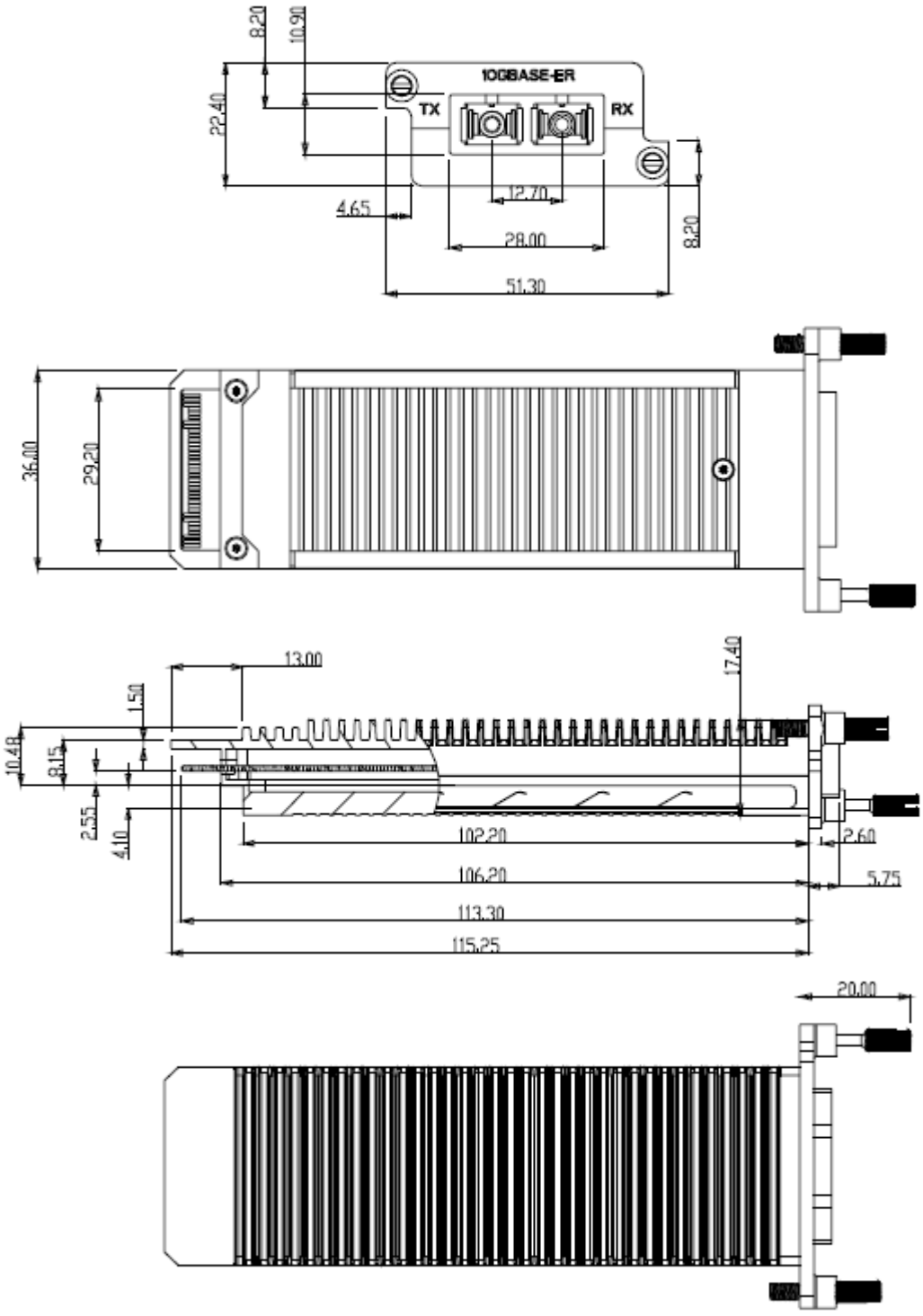
Host Board Pad Layout and Names



B. Functional Diagram

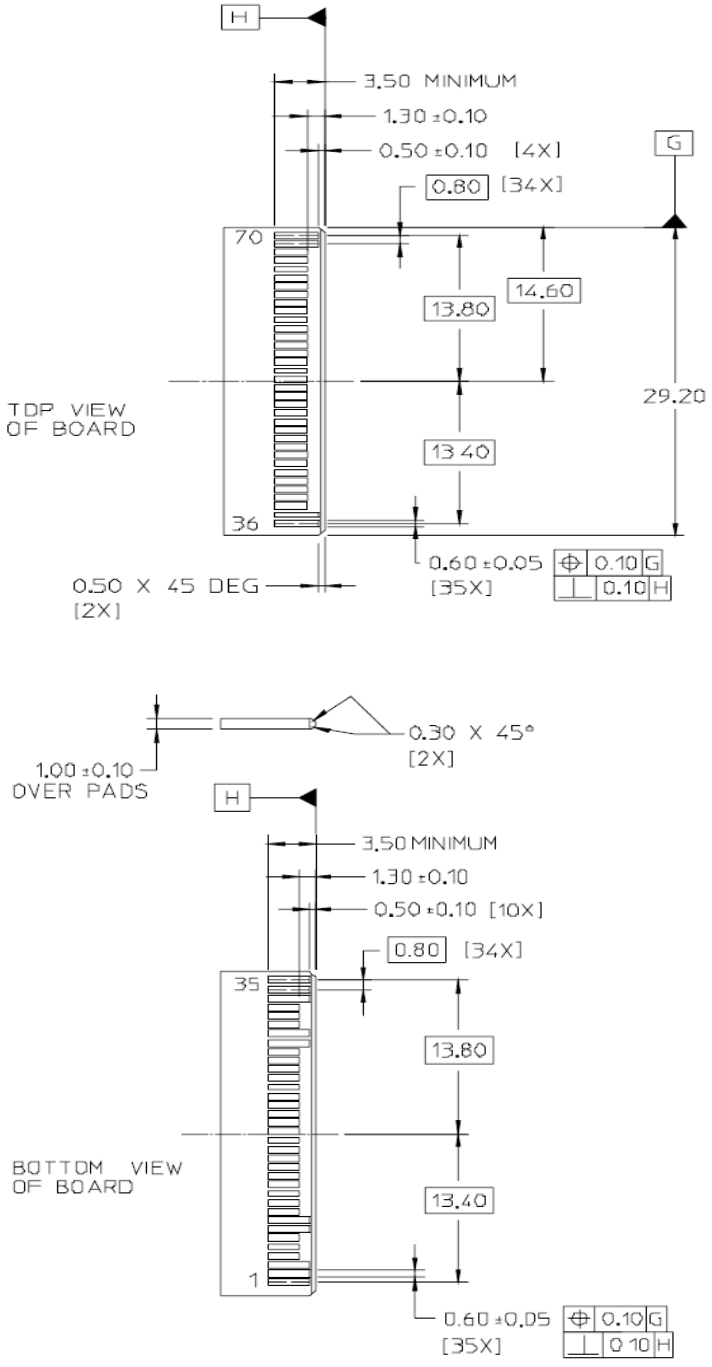


C. Package Outline

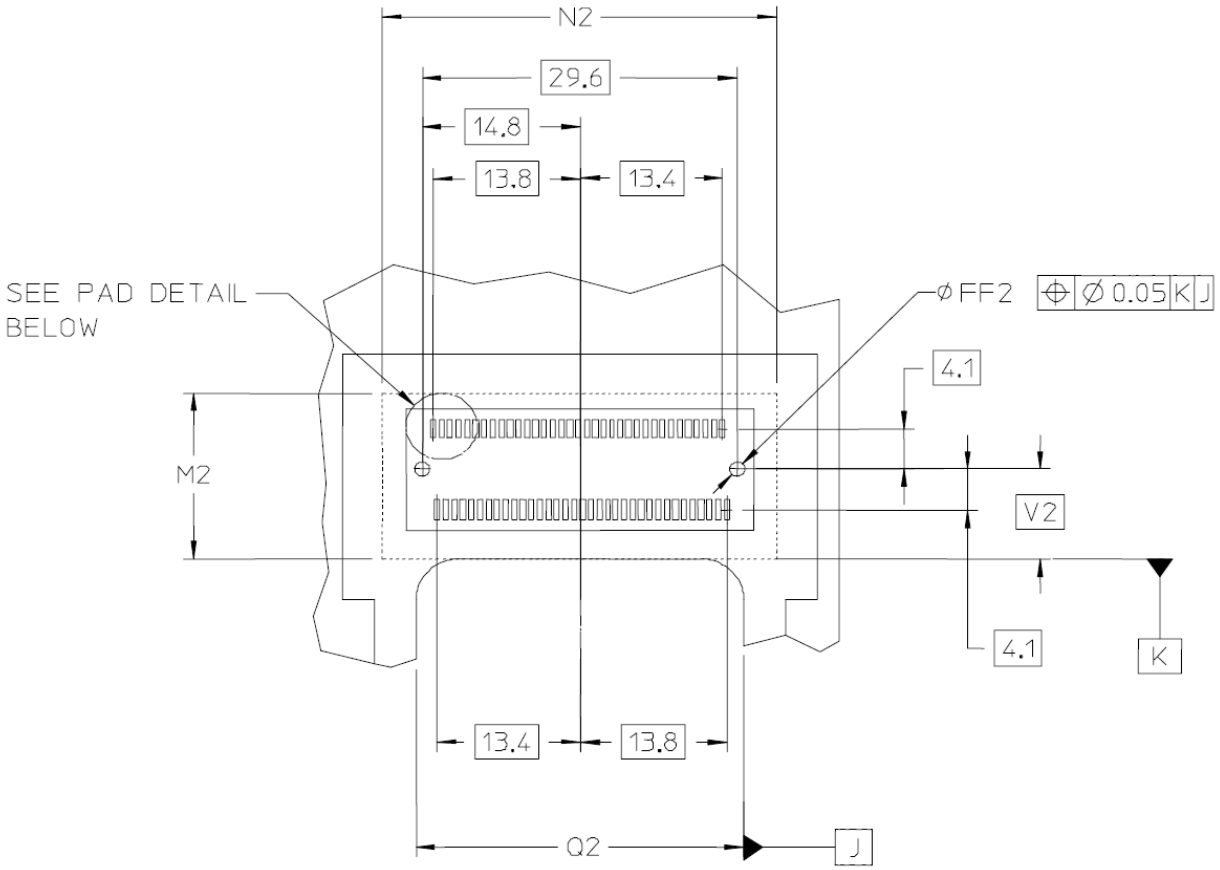


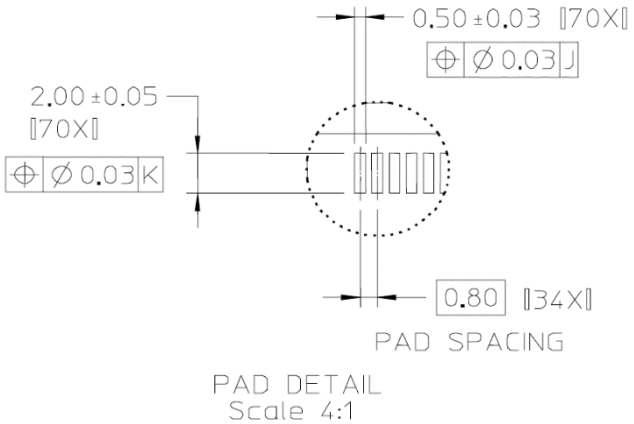
D. Transceiver and Host Printed Circuit Board

Transceiver Printed Circuit Board



Host Board Mechanical Layout





PAD DETAIL
Scale 4:1

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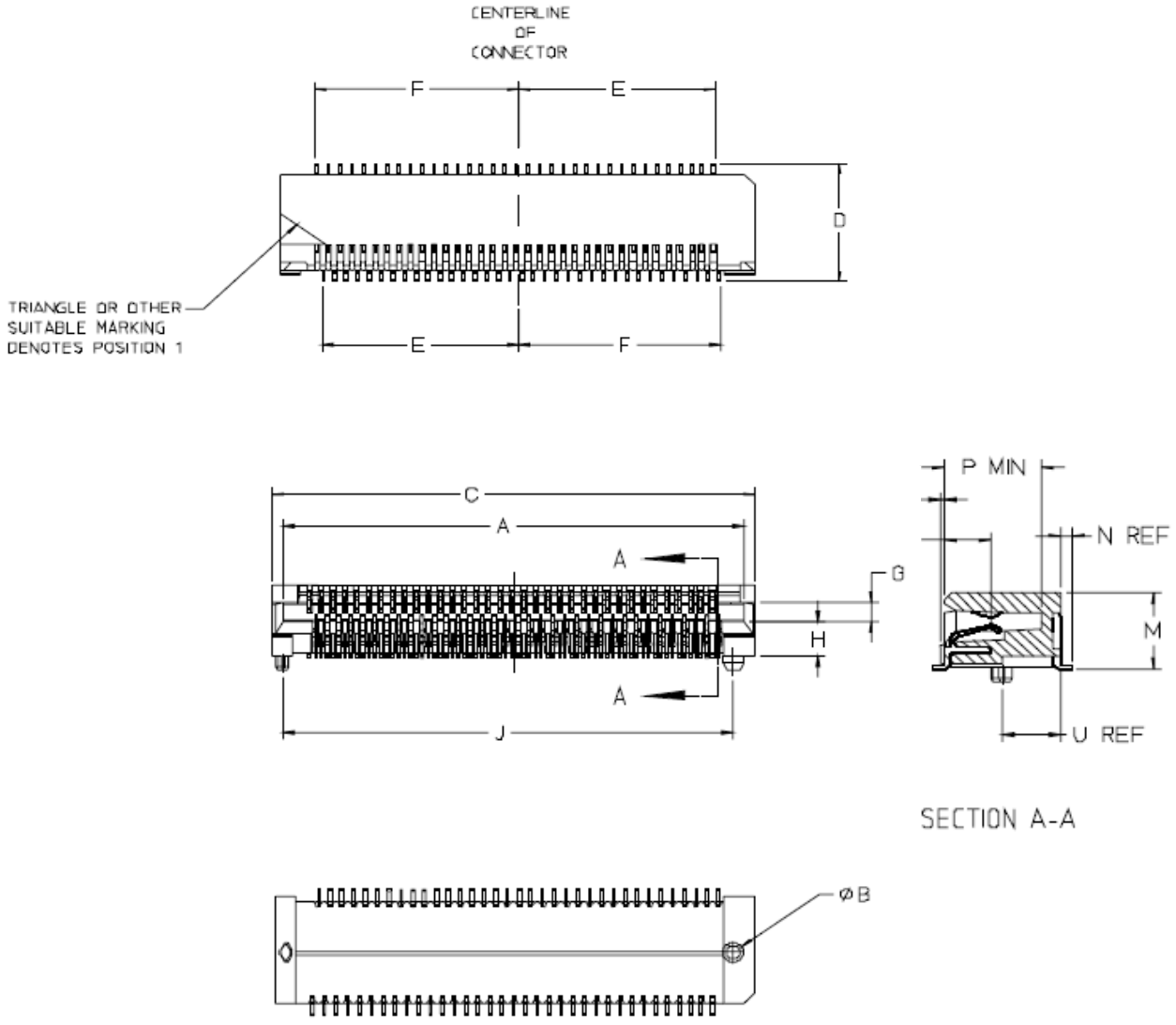
Electrical Connector



The XENPAK connector is a 70 – way two-row connector, similar in the style to the 20-way SFP connector (examples are TycoAMP Part No. 1367337 – 1 and Molex Part No. 74441-0003, or equivalent. Exact choice of connectors may depend on environment, contact manufacturer for detail.

Connector Dimensions

Key	Dim. (mm)	Tolerance	COMMENTS
A	29.4	±0.08	Connector card slot
B	1.4	±0.05	Guide pin diameter
C	31.2	Maximum	Connector width
D	9.2	Maximum	Connector Length
E	13.5	Reference	Distance from centerline of connector to outer contact
F	13.9	Reference	Distance from centerline of connector to outer contact
G	1.35	Maximum	Connector card slot height
H	2.6	Minimum	Height from bottom of connector to bottom of card slot
J	29.6	TP	Distance between guide pins
K	0.9	Reference	Diamond guide pin width, NOT SHOWN
L	1.4	±0.05	Diamond guide pin length, NOT SHOWN
M	5.9	Maximum	Connector height
N	0.8	Reference	Length of solder leads past housing, front and rear
P	6.0	Minimum	Depth of card slot from front face of housing
Q	3.0	Maximum	Depth of contact point from front face of connector
R	0.7	±0.01	Size of chamfer on top of connector, NOT SHOWN
S	0.3	Reference	Distance boss extends past front face of connector
T	0.6	Minimum	Size of chamfer at entry of card slot, all around, NOT SHOWN
U	4.5	Reference	Length from centerline of guide posts to end of solder lead

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E. Optical Interface

The objective of this section is to specify the optical connector interface sufficiently to insure performance, inter-mateability and maximum supplier flexibility.

Optical Plug

The optical interface shall use a duplex SC optical plug that conforms to IEC 61754-4. Only the floating duplex style connector plug shall be used. Rigid SC duplex connectors shall not be used. Connector keys are used to for transmit/receive polarity.

NOTE: Floating Duplex SC connectors use two simplex connectors and mechanically couple them together to create 1 connector that retains both, but allows both connectors to 'float', within the specified tolerance.

Optical Receptacle

The SC Duplex Receptacle shall conform to the requirements of IEC 61754-4 with the following clarification:

The distance between the centerline of the active optical bores shall be 12.25/13.15 mm to match the floating duplex SC optical plug. Increasing this tolerance avoids the restrictive manufacturing tolerance associated with rigid SC connectors.

F. Mechanical Forces

This following limits should be observed when designing for, or using. XENPAK transceivers:

Maximum insertion force = 80 N
(Includes connector, interposer and connector shield ground spring)

Maximum extraction force = 50 N

Maximum retention force (with screws engaged) = 130 N

Fastener Torque: 0.1 Nm (3 mm captive screw)

G. Transceiver and Connector Durability

The following life ratings should be observed when designing for, or using, XENPAK transceivers and their associated connectors.

Minimum mate/de-mate cycles for transceiver = 50 cycles

Minimum mate/de-mate cycles for 70-pin connector = 100 cycles

H. XENPAK Thermal Requirements

Maximum Power Dissipation

Transceivers with 850nm or 1310nm PMD will dissipate a maximum of 6 W.

Transceivers with 1550nm PMD will dissipate a maximum of 10 W.

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Maximum Case Temperature

Maximum case temperature for a XENPAK module is 70 C. Case temperature is as defined in IEC 60950 section 4.5.1 and table 4B.

Maximum case temperature of 70 C is specified for systems with 8 or fewer adjacent 850nm or 1310nm modules.

Maximum case temperature of 70 C is specified for systems with 4 or fewer adjacent 1550nm modules.

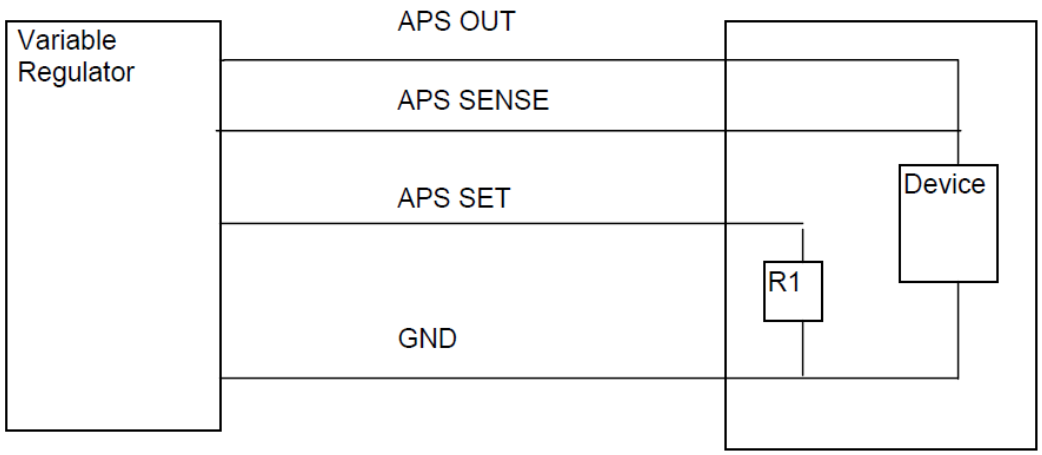
Case temperature is not specified for systems with mixed PMD types (850/1310/1550nm). Individual characterization of systems with mixed PMD types is recommended.

I. XENPAK Electrical Interface

Power Supplies and Hot Swapping

5.0V, 3.3V, and an Adaptable Power Supply rail (APS) should be supplied to a XENPAK transceiver through the transceivers connector. During module insertion chassis ground connects first to the customer chassis via the chassis areas defined in the following figure on the host board. The first electrical connector pins to make the contact are Electrical Ground and APS power followed by VCC and Signal contacts. The 10G transceiver should tolerate biasing of signal contacts in the absence of VCC.

Adaptable Power Supply



The Back-plane will provide an adaptable power supply capable of adjusting from a high of 1.8 volts to a low 0.9 volts.

The XENPAK module shall support a voltage sense pin for the APS on the "APS Sense" pin. The XENPAK module shall incorporate a resistor R1, between the "APS Set" pin and ground. Resistor values, corresponding to the required voltage.

If the pin used for APS SET is shorted to ground on the module, the APS will default to a fixed 1.8 volts.

The signal contact pin #14 "MOD DETECT" may be used to enable the APS power when the module is installed. The host design may also take control of the APS supply enable pin via software or some other mechanism.

The Adaptable supply can compensate for undesired voltage drops across the host PCB the XENPAK connector and potentially inside the XENPAK module itself (implementation dependent).

Because the APS sense does not compensate for voltage drops on the ground plane and ground pins of the connector, it is important that the ground path has a very low voltage drop, 1% is used in the tolerance analysis.

The host will provide < 200 mV to the adaptable voltage rail when no XENPAK module is installed and will ramp up to the requested voltage and be within specification within 500 ms of full insertion.

The APS is intended to default to a low voltage output if any single pin makes a poor connection, specifically:

If the APS SET pin is connected and the APS Sense pin is open, the APS supply will put out near zero volts due to the 500 Ohm pull-up resistor to 3.3 volts.

▪If the APS Sense is connected and the APS SET connection is open, the supply defaults to low voltage of 0.8 volts.

▪ If both the APS SET and APS Sense connections are open, the APS supply will put out near zero volts.

▪The APS supply leads are elongated to prevent a condition where the SENSE lead connects before the APS supply leads and pulls down the SENSE pin resulting in an instantaneous high voltage from the APS, before the module is fully seated.

Adaptable Power Supply Reference

The APS supply on the host will regulate the APS voltage such that the voltage on the network labeled "Vfeedback" becomes nominally 0.8 volts unless an APS voltage or current limiting conditions takes priority. The resistors in the following table are calculated using resistors available as 1% values. For tolerance purposes, it is recommended that 0.1% resistors are used to provide additional tolerance margin although 1% may be suitable for some applications. These values are subject to change after a host back-plane is built and tested.

Resistor Values for APS Operation

V_{nom} volts	R1 Ohms
0.9	6810
1	3160
1.1	1820
1.2	1180
1.3	806
1.4	536
1.5	348
1.6	210
1.7	97.6
1.8	0

The resistor values given in the above Table place the nominal set-point slightly high, to help compensate for some of the anticipated ground plane drop.

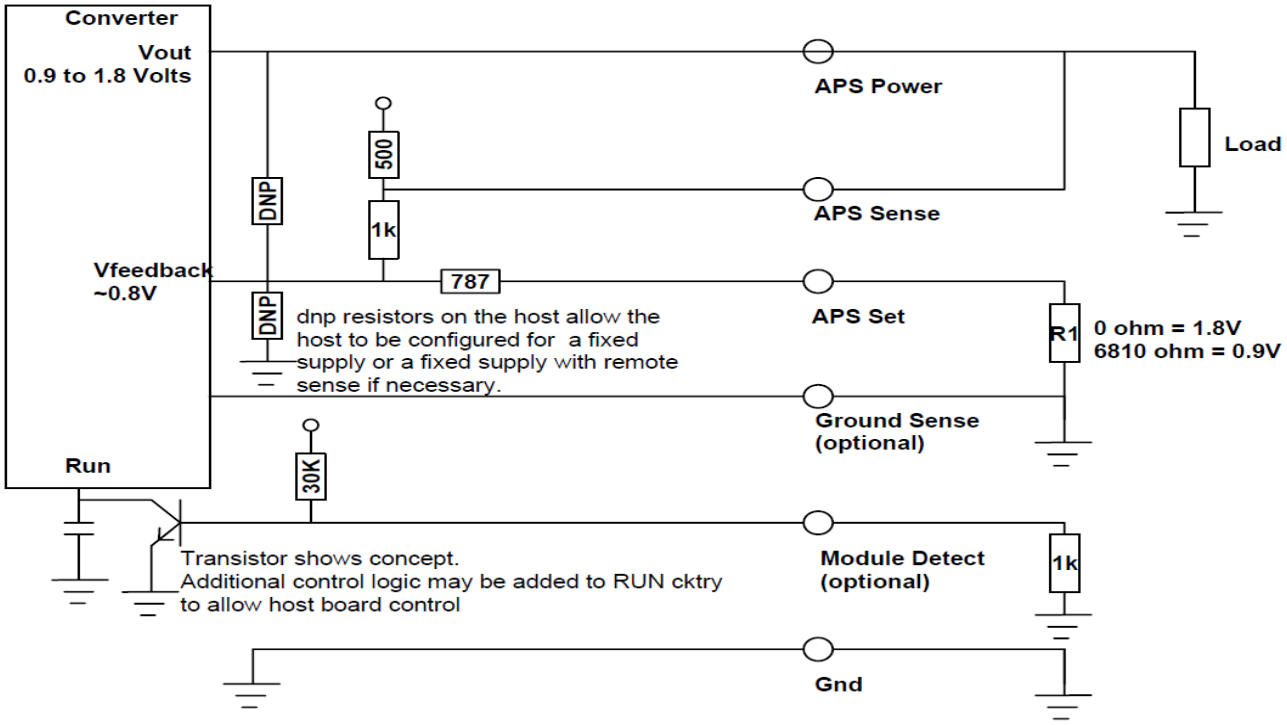
Recommended Tolerance (+/-)

Supply Precision	1.5%
Supply Load Regulation	0.3%
Ground Plane and Ground Connector Drop	1.0%
Resistor Tolerance using 0.1% parts	0.3%
Margin	0.9%
Total APS Tolerance (+/-)	4.0%

Voltage Calculation

The circuit BELOW depicts conceptually the design used to generate the APS voltage. Exact implementation and component values are not mandatory on the host. The APS implementer is responsible for ensuring that the XENPAK module is supplied in a manner which conforms to the APS tolerance states for any given resistance between the module set pin and module ground.

APS Schematic



Current Capability of the APS

The APS will provide from 0.1 to 1.8 amperes and will current limit at typically 2 to 4 amperes.

Adaptable Power Supply Specs/Requirements

The host PCB will provide a steady state voltage on the adaptable voltage power conforming to the specifications.

APS Tolerance (+/-)

APS steady state RMS ripple	<40mV rms
APS tolerance for a given resistance from APS set to the ground	+/- 3%
APS max overshoot after insertion/host power up	3% of V steady state
APS min rated current	0.1 Amps
APS maximum rated current for any voltage	1.8 Amps
APS current limit	2 -> 4 Amps
XENPAK total capacitance of transceiver APS power pins	<200 uF

J. Fixed Voltage Supply Specs and Inrush Currents

These specifications shall be applicable to the fixed 3.3V and 5.0V supply rails. The inrush current on any fixed supply rail during hot plug or power up in host of a XENPAK module shall be limited by the XENPAK module to assure a maximum rate of change defined in Table 7. The peak inrush currents to any supply rail shall not exceed the steady state currents for that rail by more than 50%.

Ramp up time controlled by the XENPAK module shall allow operation within 5 seconds after the adaptable power supply back-plane has stabilized as required above.

Fixed Power Rail Tolerance (+/-)

Steady State Voltage Accuracy	+/- 5% or rated
Steady state RMS ripply (max)	40 mV rms
Stabilization time to rated tolerance (max)	< 500 ms
Inrush current during hot plug max	50 mA/ms
Inrush current (per power pin) max	< 0.75A (150% x 0.5A steady state rating)

A XENPAK module inserted in this system shall inject < 20mV rms ripple onto any fixed voltage rail when supplied from a "near ideal" voltage source followed by a 5 ohm series resistor.

Hot Swap and Transceiver Power-On-Reset Definition

When a 10G transceiver is inserted the ramp rate of supply current must also comply with the specification. Control of inrush current should be internal to the XENPAK transceiver.

The 10G transceiver shall achieve a stable state of normal operation after mechanical insertion at time, t = 0 according to the following specification.

Power on Reset Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units
Icc Peak Inrush	IccPEAK	-	-	50	%
Icc Ramp Rate	dICC/dt	-	-	50	mA/ms
Initialization Time	Tinit	-	-	5	s

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Low Power Start-up (LPS) Mode

Low power startup is an optional feature of XENPAK modules. A transceiver will indicate it's LPS ability by setting bit 0 of the Optional Capability Register to 1 if implemented and 0 otherwise.

If LPS is implemented the module will only initialize the MDIO-functionality, and limit the power consumption to a fraction of normal levels, typical less than 1W.

For LPS to be invoked, the system shall pull the signal TX ON/OFF (pin 12) low, for all the empty module slots and hot it low after a module is inserted, until the system reads the modules registers and establishes what it's respective thermal and power needs. The system can thereby establish if the newly inserted module causes it to exceed it's thermal or power supply capacity and to reject the module, by holding it in a low power state until it does. Otherwise the system enables the module to commence normal operation, by raising the TX ON/OFF signal.

The XENPAK NVR contains pre-programmed power supply requirement information for an LPS enabled module.

The LPS feature is particularly relevant to longer reach XENPAKs which may load power supplies and cooling more than shorter reach parts, but which are not typically inserted into all ports of a line card.

Four measurements are made on a representative sample of part of a representative build standard in the MSA thermal test chamber.

Specific parameters are:

- 5V Stressed Environment Reference (100% = 1A)
- 3,3V Stressed Environment Reference (100% = 2A)
- APS Stressed Environment Reference (100% = 2A)
- Nominal APS Voltage

Under the following conditions:

One module is inserted in the test fixture middle slot (number four or five) with the remaining front openings closed with blanking plates. An inlet air temperature of 50 C and airspeed of 2 m/s shall be used for the single stressed environment current reference measurement on each rail.

Initialization and Reset

After successful plug in and initialization sequence the transceiver should clear MDIO Bit register N.0.15 (Where N = any implemented device). A timing diagram is shown below. The transceiver may be reset in situ using the hardware reset pin or MDIO register bit 1.0.15.

When reset using the hardware reset pin or by setting Bit 15 in MDIO register 1.0 the transceiver should initialize and then MDIO Bit N.0.15.

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K. Transceiver Monitoring

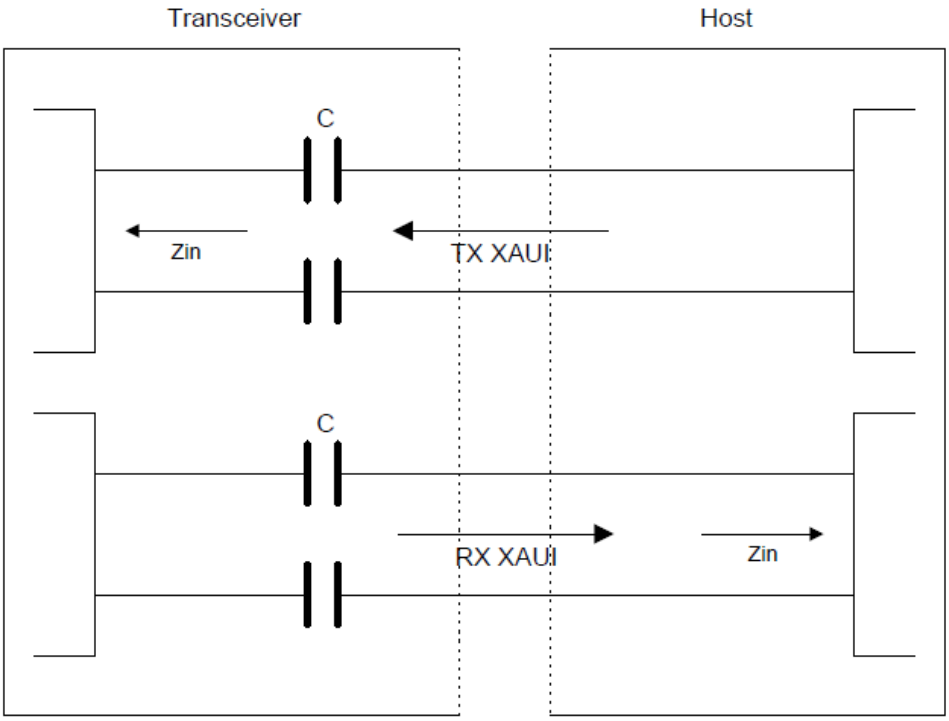
Contacting are available on the module connector for Link Alarm Status Interrupt (LASI). A module detect pin allows hardware detection of a module when it is inserted into a customer chassis. This pin is pulled through 1kW to GND inside the module and can be used to drive an interrupt for polling-free module detection.

The 2-wire Management Data I/O interface (802.3ae Clause 45) is mandatory in the XENPAK MSA. MDC provides clocking for the data that is passed on the MDIO line. Five further pins allow for loading of a Port Address (PRTAD0-4) into the module.

High Speed Signals

The XAUI transmit and receive data complies with IEEE802.3ae Clause 47 electrical specification, which should be referenced for actual values. AC coupling is provided inside the module for both transmit and receive directions as indicated in the following figure. For clarity only one TX and RX XAUI lane is shown. The impedance of Zin is 100 Ohms differential.

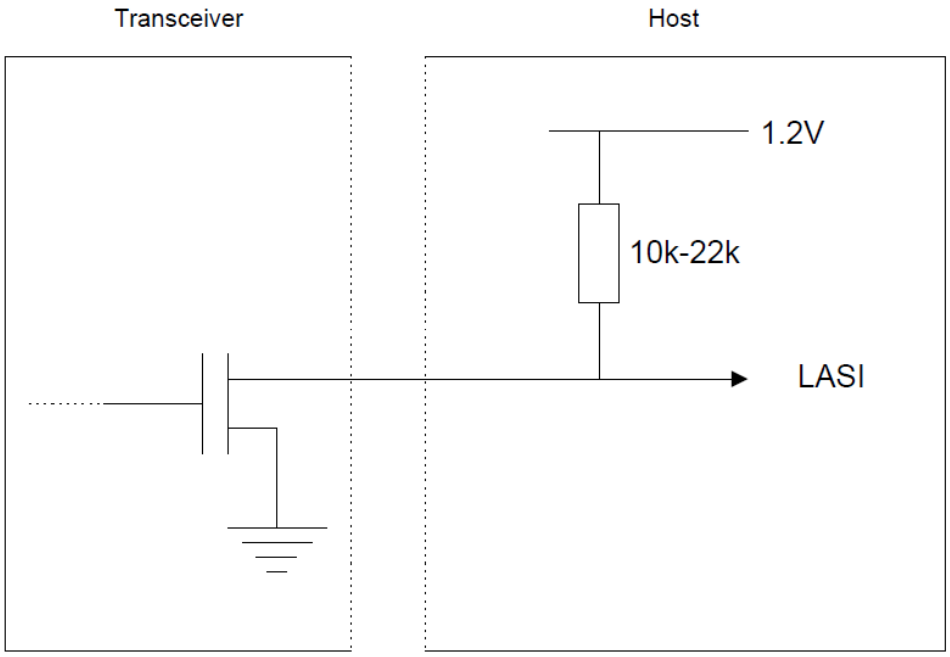
High Speed Signals



Low Speed Signals

Low Speed Signals, as indicated in the following Table, are open drain compatible to permit wired 'OR' connections. Pull up resistors are provided in the transceiver or on the host board according to the following figure.

Example of Low Speed Output Configuration



Example of Low Speed Output Configuration

Parameter	Min	Typ	Max	Units	Notes
VIL(Max)	-	-	0.36	V	1.2V CMOS
VIH(Min)	0.84	-	1.25	V	1.2V CMOS
Capacitance	**-**	-	320	pF	Maximum Fan-out of 32. 10pF per port
Pull Up Resistance	10k		22k	Ω	

Initialization and Reset

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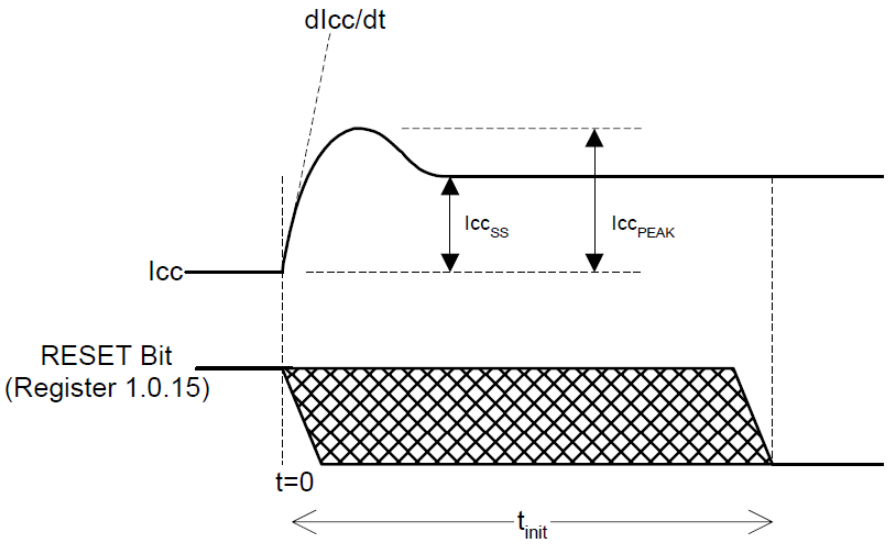
When reset using the hardware reset pin or by setting Bit 15 in MDIO register 1.0 the transceiver should initialize and then MDIO Bit N.0.15.

Initialization and Hot Swap Timing Diagram



Relationship between the TRANSCEIVER RESET pin and MDIO Reset Bit

RESET Pin	MDIO Register Condition 1.0.15	Transceiver Behavior
1	0	Normal Operation
0	0	Transient state between RESET PIN low and 1.0.15 getting set
1	1	Reset State
0	1	State assumed shortly after Transceiver reset pin pulled low

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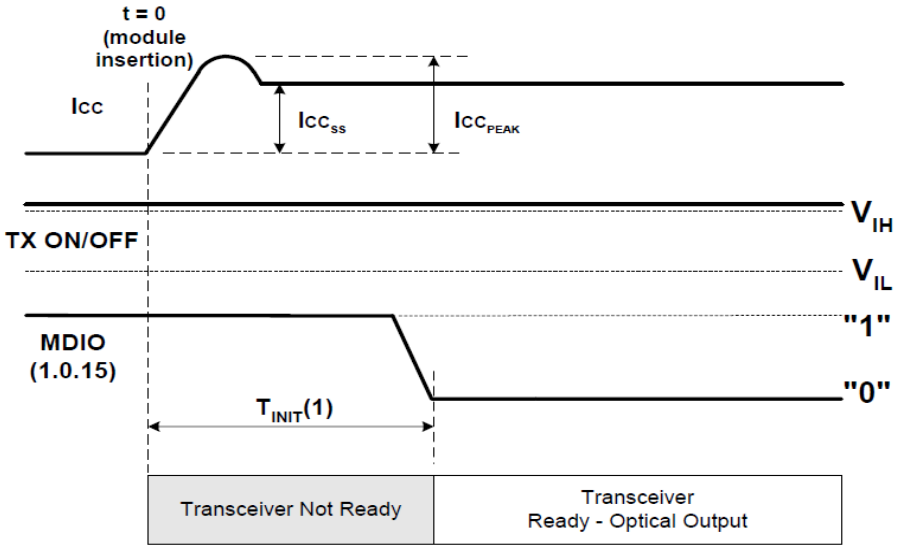
Tx On/Off

The timing relationship between Tx on/off and the optical output is shown below, The optical output will turn off within 100us Tx ON/OFF being pulled low.

Tx Off to Optical Output Timing, Normal Operation



Tx Off to Optical Output Timing