

1x9 SC Bi-Directional (BiDi) Optical Transceivers

Introduction

This design guide provides the information needed to incorporate OptixCom's fiber optics transceiver products in the customer's system. This guide will focus on the 1x9 BiDi products with the single SC connector interface.

The reference guide covers the following topics:

- A. Pin Assignment & Description
- B. Recommended Interface Circuit
- C. Host Board Mechanical Layout
- D. Package Outline



A. Pin Assignment & Description

Top View		
○ 1	RX GND	○
○ 2	RD+	○ NC
○ 3	RD-	
○ 4	SD	
○ 5	RX Vcc	
○ 6	TX Vcc	
○ 7	TD-	
○ 8	TD+	○ NC
○ 9	TX GND	○

PIN	Symbol	Description
1	RX GND	Receiver Ground
2	RD+	Receiver Data Output +
3	RD-	Receiver Data Output -
4	SD	Signal Detect
5	RX Vcc	Receiver Power Supply
6	TX Vcc	Transmitter Power Supply
7	TD-	Transmitter Data In -
8	TD+	Transmitter Data In +
9	TX GND	Transmitter Ground

TD+, TD-: AC/DC coupled LVPECL inputs for the transmitter. Two 50Ω differential lines.

RD+, RD-: Open-emitter out circuits. AC/DC coupled LVPECL outputs for the receiver. Two 50Ω differential lines.

SD: Signal Detect. Normal optical input levels to the receiver result in a logic "1" output, V_{OH} , asserted. Low input optical levels to the receiver result in a fault condition indicated by a logic "0" output V_{OL} , deasserted. It is a single-ended LVPECL/LVTTL output.

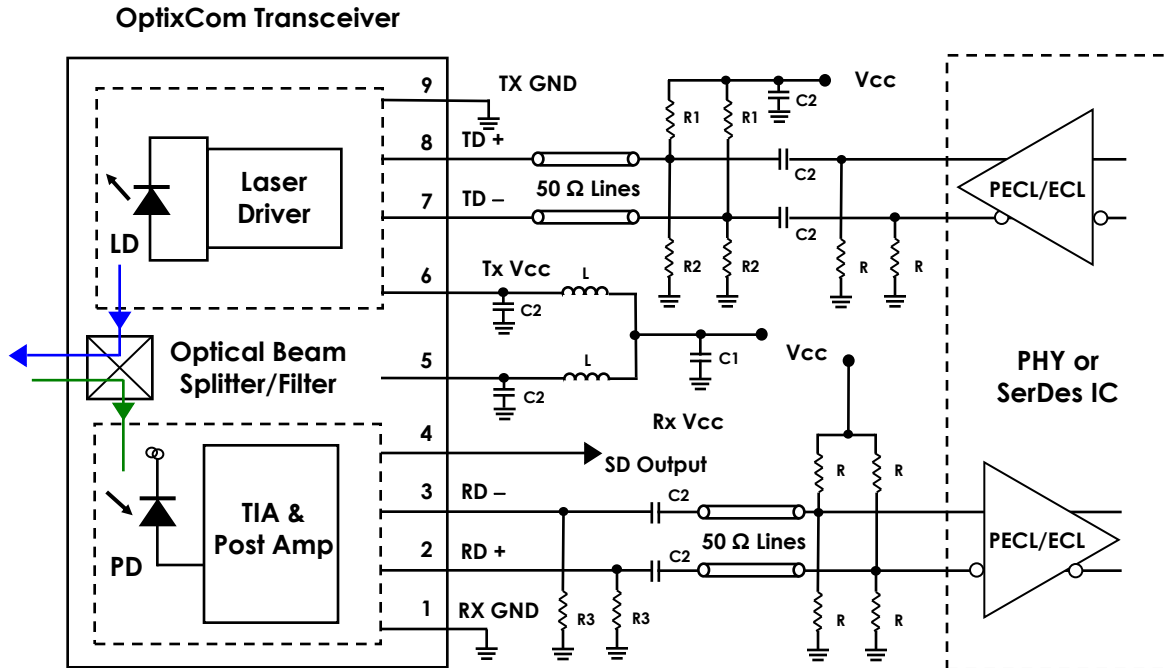
For TTL output of SD, it is an open collector/drain output, which should be pulled up with a 4.7K - 10K resistor. Pull up voltage between 2.0V and TX Vcc. Connect to ground if not needed.

For LVPECL output of SD, and can be terminated with LVPECL techniques via 50 Ω to RX Vcc - 2V. Connect to ground if not needed.

Alternatively, SD can be loaded with a 180 Ω resistor to RX GND to conserve electrical power with small compromise to signal quality. If SD output is not used, leave it open-circuited. This SD output can be used to drive a LVPECL input on an upstream circuit, such as, SD input or Loss of Signal-bar. Connect to ground if not needed.

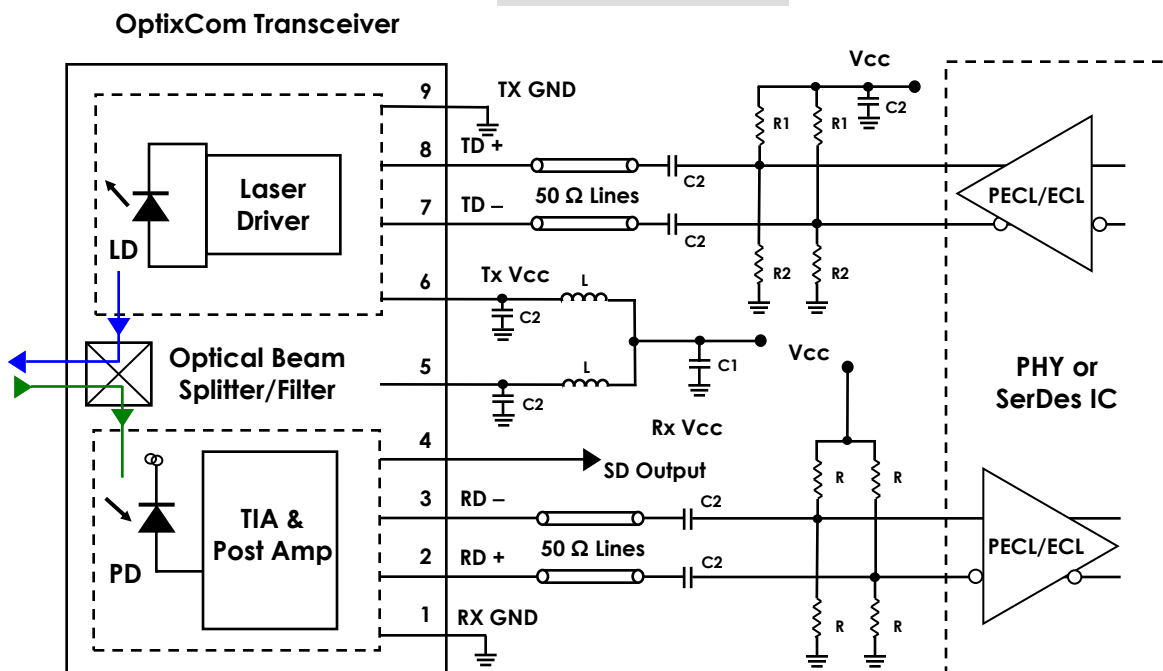
B. Recommended Interface Circuit

DC Coupling I/Os

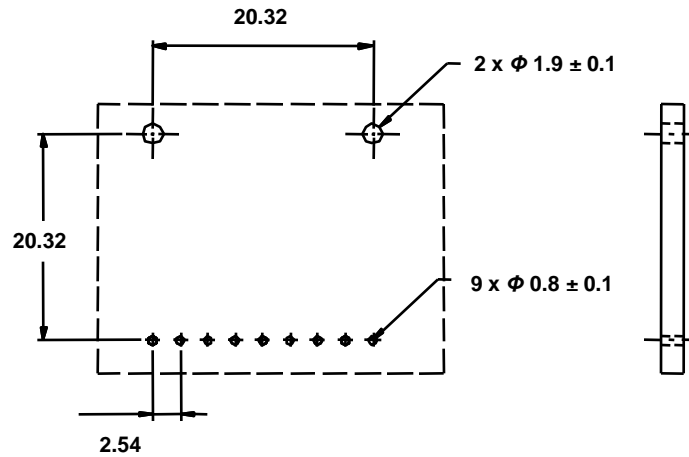


C1: 4.7 μ F, C2: 100 nF, L: 1 μ H, R1: 82 Ω , R2: 130 Ω , R3: 180 Ω , R: depends on SerDes IC

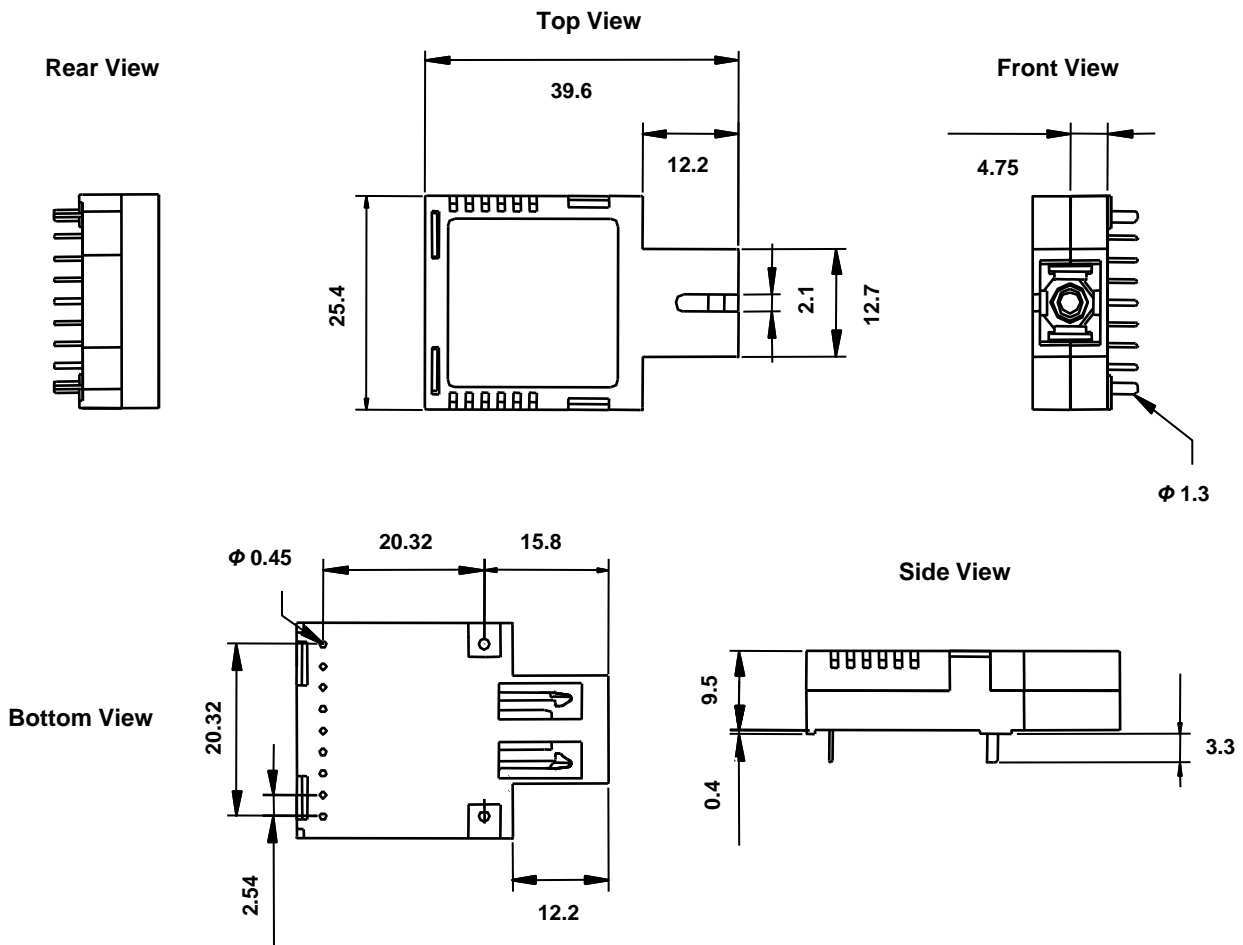
AC Coupling I/Os



C. Host Board Mechanical Layout



D. Package Outline



Unit: mm, typical tolerance for these dimensions is ± 0.1 mm